Rejection of Claims under 35 USC §102

Claims 1-6, 16-19, 21, 29-32, 36, 39-43, 49-51, and 57 are rejected under 35 USC §102(e) as being anticipated by U.S. Patent No. 6,289,414 to Feldmeier et al (Feldmeier). Applicants respectfully traverse these rejections.

Claims 1-28

Applicants' Claim 1 recites:

> A content addressable memory (CAM) system including an array of binary CAM cells segmented into a plurality of array groups, each array group having a group global mask for storing a mask pattern indicating priority of the array group.

Feldmeier neither discloses nor suggests the CAM device recited in Applicants' Claim 1.

Feldmeier discloses storing address entries in a CAM array according to mask or priority number so that address entries having the same mask number are grouped together, with the addresses having the highest mask numbers stored in the lowest CAM addresses (see col. 10, lines 55-65). A sorting algorithm is required to maintain proper ordering of the groups of address entries (see col. 11, lines 50-65 and col. 14, lines 28-41). Each group of address entries in Feldmeier's CAM array corresponds to an address space that is defined by a "Floor" address and a "Blocksize" parameter (see col. 15, lines 1-35). The address space assigned to each group of entries can be changed to make room for more entries by adjusting the group's Floor address and/or Blocksize parameter, thereby "shifting" the group of entries to a new address space (see col. 15, line 53 to col. 16, line 2). The IP mask numbers are logically combined with IP addresses when the address entries are stored in the CAM array, thereby encoded mask information within each address entry (see col. 12, lines 55-67). A single mask register 40 is provided for Feldmeier's entire CAM array (see col. 13, lines 2- 27 and FIG. 20).

Feldmeier fails to disclose or suggest that each array group includes a global mask that stores a mask pattern indicating the array group's priority. Rather, as mentioned above, Feldmeier discloses only one mask register 40 for the entire CAM. Further, in contrast to Applicants' Claim 1, Feldmeier stores mask information (e.g., priority numbers) within each address entry stored in the CAM, not within a global mask for each group. Thus, while Applicants' Claim 1 recites "each array group having a group global mask for storing a mask pattern indicating priority of the array group," Feldmeier teaches that "the individual addresses

Accordingly, because Feldmeier fails to disclose or suggest "an array of binary CAM cells segmented into a plurality of array groups" or "a priority table including a plurality of rows, each for storing the priority of a corresponding array group," as recited in Claim 29, Claim 29 is neither anticipated nor rendered obvious by Feldmeier.

Claims 30-38 depend from Claim 29 and therefore distinguish over the cited references for at least the same reasons as Claim 29.

Claims 39-57

Claim 39 (as amended) recites:

A method of operating a content addressable memory (CAM) system including an array of binary CAM cells segmented into a plurality of array groups, comprising:

assigning a priority to one or more array groups; and

selectively storing data in the array groups according to priority, wherein assigning the priority comprises:

for each array group, storing a mask pattern indicative of the priority assigned to the array group in a global mask for the array group.

As discussed above with respect to Claim 1, Feldmeier fails to disclose or suggest "storing a mask pattern indicative of the priority assigned to the array group in a global mask for the array group," as recited in Claim 39. Therefore, Feldmeier neither anticipates nor renders obvious Applicants' Claim 39.

Claims 40 and 42-57 depend from Claim 39 and therefore distinguish over the cited references for at least the same reasons as Claim 39.

Rejection of Claims under 35 USC §103

Claims 20, 22-26, and 48 are rejected under 35 USC §103(a) as being unpatentable over Feldmeier in view of USP 4,928,260 to Chuang et al (Chuang). Applicants respectfully traverse these rejections.

Claims 20 and 22-26 depend from Claim 1, and therefore distinguish over the cited references for at least the same reasons as Claim 1.

Accordingly, because Feldmeier fails to disclose or suggest "an array of binary CAM cells segmented into a plurality of array groups" or "a priority table including a plurality of rows, each for storing the priority of a corresponding array group," as recited in Claim 29, Claim 29 is neither anticipated nor rendered obvious by Feldmeier.

Claims 30-38 depend from Claim 29 and therefore distinguish over the cited references for at least the same reasons as Claim 29.

Claims 39-57

Claim 39 recites:

A method of operating a content addressable memory (CAM) system including an array of binary CAM cells segmented into a plurality of array groups, comprising:

assigning a priority to one or more array groups; and

selectively storing data in the array groups according to priority, wherein assigning the priority comprises:

for each array group, storing a mask pattern indicative of the priority assigned to the array group in a global mask for the array group.

As discussed above with respect to Claim 1, Feldmeier fails to disclose or suggest "storing a mask pattern indicative of the priority assigned to the array group in a global mask for the array group," as recited in Claim 39. Therefore, Feldmeier neither anticipates nor renders obvious Applicants' Claim 39.

Claims 40 and 42-57 depend from Claim 39 and therefore distinguish over the cited references for at least the same reasons as Claim 39.

Rejection of Claims under 35 USC §103

Claims 20, 22-26, and 48 are rejected under 35 USC §103(a) as being unpatentable over Feldmeier in view of USP 4,928,260 to Chuang et al (Chuang). Applicants respectfully traverse these rejections.

Claims 20 and 22-26 depend from Claim 1, and therefore distinguish over the cited references for at least the same reasons as Claim 1.

Claim 48 depends from Claim 39, and therefore distinguishes over the cited references for at least the same reasons as Claim 39.

New Claims 58 and 59

Claim 58 depends from Claim 1, and therefore distinguishes over the cited references for at least the same reasons as Claim 1.

Claim 59 depends from Claim 31, and therefore distinguishes over the cited references for at least the same reasons as Claim 31.

New Claims 60-72

Independent Claim 60 recites:

A content addressable memory (CAM) comprising:

a plurality of CAM array groups each including a plurality of rows of binary CAM cells; and

a plurality of group global mask circuits each coupled to a corresponding one of the CAM array groups and each for storing a group global mask for globally masking one or more bits in all of the rows of CAM cells of the corresponding CAM array group, wherein each group global mask indicates a priority of the corresponding group of CAM cells relative to other CAM array groups.

As discussed above with respect to Claim 1, Feldmeier fails to disclose or suggest "a plurality of group global mask circuits each coupled to a corresponding one of the CAM array groups and each for storing a group global mask for globally masking one or more bits in all of the rows of CAM cells of the corresponding CAM array group," as recited in Claim 60, and therefore neither anticipates nor renders obvious Claim 60.

Claims 61-72 depend from Claim 60, and therefore distinguish over the cited references for at least the same reasons as Claim 60.

New Claims 73-84

Independent Claim 73 recites:

A content addressable memory (CAM) comprising:

a plurality of CAM array groups each including a plurality of rows of binary CAM cells; and

means for assigning a first priority to a first and a second of the CAM array groups, and for assigning a second priority to a third of the CAM array groups, wherein the first and second priorities are different, and wherein the third CAM array group occupies an address space numerically between address spaces occupied by the first and second CAM array groups.

Feldmeier fails to disclose or suggest "means for assigning a first priority to a first and a second of the CAM array groups, and for assigning a second priority to a third of the CAM array groups, wherein the first and second priorities are different, and wherein the third CAM array group occupies an address space numerically between address spaces occupied by the first and second CAM array groups," as recited in Claim 73, and therefore neither anticipates nor renders obvious Claim 73. In contrast, Feldmeier teaches storing entries in a CAM array such that address entries having the highest mask numbers are stored in the lowest CAM addresses and address entries having the lowest mask numbers are stored in the highest CAM addresses (see col. 10, lines 55-65).

Claims 74-84 depend from Claim 73, and therefore distinguish over the cited references for at least the same reasons as Claim 73.

New Claims 85-88

Independent Claim 85 recites:

A content addressable memory (CAM) comprising:

a plurality of CAM array groups each including a plurality of rows of binary CAM cells each coupled to a corresponding match line;

a plurality of group global mask circuits each coupled to a corresponding one of the array groups and each for storing a group global mask for globally masking one or more bits in all of the rows of binary CAM cells of the corresponding array group; and

an index circuit coupled to the match lines to determine, as between rows of CAM cells in different array groups that contain data matching a search key as masked by their corresponding group global masks, an index of one of the rows of CAM cells that contains the

data matching the search key, wherein one of the rows of CAM cells has a corresponding group global mask that masks fewer bits than the other group global masks associated with the other rows of CAM cells that store data matching the search key.

As discussed above with respect to Claim 1, Feldmeier fails to disclose or suggest "a plurality of group global mask circuits each coupled to a corresponding one of the array groups and each for storing a group global mask for globally masking one or more bits in all of the rows of binary CAM cells of the corresponding array group," as recited in Claim 85, and therefore neither anticipates nor renders obvious Claim 85.

Claims 86-88 depend from Claim 85, and therefore distinguish over the cited references for at least the same reasons as Claim 85.

CONCLUSION

In light of the above amendments and remarks, it is believed that Claims 1-40 and 42-88 are in condition for allowance and, therefore, a Notice of Allowance of Claims 1-40 and 42-88 is respectfully requested. If the Examiner's next action is other than allowance as requested, the Examiner is requested to call the undersigned at (415) 291-9497.

Respectfully submitted,

Dated: April 21, 2003

William L Paradice III
Reg. No. 38,990

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on April 21, 2003.

By: _____
William L Paradice III